WHAT IS CLAIMED IS:

1. An apparatus comprising:

an electromagnetic shielding structure formed at least partially in one or more redistribution layers formed on an integrated circuit die, the electromagnetic shielding structure substantially surrounding a circuit element.

2. The apparatus as recited in claim 1 wherein the circuit element is formed at least partially in the one or more redistribution layers.

3. The apparatus as recited in claim 1 wherein the redistribution layers are formed above a passivation layer of the integrated circuit die.

4. The apparatus as recited in claim 1 wherein the redistribution layers are formed above integrated circuit pads.

5. The apparatus as recited in claim 1 wherein the circuit element is formed below a passivation layer of the integrated circuit die.

6. The apparatus as recited in claim 1 wherein the electromagnetic shielding structure has a top plate, a bottom plate, and sidewalls.

7. The apparatus as recited in claim 6 wherein the circuit element is substantially equidistant between the top and bottom plates.

8. The apparatus as recited in claim 6 wherein the circuit element is positioned between the top and bottom plates based at least in part on resistivities of the top and bottom plates.

9. The apparatus as recited in claim 6 wherein at least one of the top plate or bottom plate of the electromagnetic shielding structure is formed in under bump metal.

10. The apparatus as recited in claim 6 wherein the sidewalls of the electromagnetic shielding structure are formed at least in part by under bump metal.

11. The apparatus as recited in claim 6 wherein the top plate and at least a portion of the sidewalls are formed by under bump metal.

12. The apparatus as recited in claim 11 wherein the top plate is supported by via structures formed in the redistribution layers.

13. The apparatus as recited in claim 6 wherein the sidewalls of the electromagnetic shielding structure are formed at least in part by via structures in the integrated circuit die.

14. The apparatus as recited in claim 13 wherein the sidewalls of the electromagnetic shielding structure are formed at least in part by solid via structures in the redistribution layers.

15. The apparatus as recited in claim 6 wherein the sidewalls of the electromagnetic shielding structure are formed at least in part by discrete via structures in the redistribution layers.

16. The apparatus as recited in claim 15 wherein the discrete via structures in the redistribution layers are stacked.

17. The apparatus as recited in claim 15 wherein the discrete via structures in the redistribution layers are staggered.

18. The apparatus as recited in claim 1 wherein the redistribution layers include at least one redistribution metal layer and at least one redistribution dielectric layer.

19. The apparatus as recited in claim 18 wherein the redistribution dielectric layer is at least 5um thick and a dielectric layer of the integrated circuit die is less than 1um thick.

20. The apparatus as recited in claim 19 wherein the redistribution dielectric layer is at least 15 um thick.

21. The apparatus as recited in claim 1 wherein the circuit element comprises an inductor structure.

22. The apparatus as recited in claim 21 wherein the inductor structure comprises a parallel-connected pair of inductor loops.

23. The apparatus as recited in claim 22 wherein current flow through the pair of inductor loops is substantially balanced.

24. The apparatus as recited in claim 22 wherein the pair of inductor loops are formed in a planar configuration.

25. The apparatus as recited in claim 22 wherein the pair of inductor loops are formed in a vertical configuration.

26. The apparatus as recited in claim 21 wherein the inductor structure comprises a series-connected pair of inductor loops.

27. The apparatus as recited in claim 21 wherein the electromagnetic shielding structure substantially surrounds at least one capacitor coupled in parallel with the inductor structure.

28. The apparatus as recited in claim 21 wherein at least one amplifier circuit is coupled in parallel with the inductor structure.

29. A method comprising:

electromagnetically shielding at least one circuit element formed on an integrated circuit die by substantially surrounding the circuit element with an electrically conductive enclosure formed at least partially in one or more redistribution layers formed on the integrated circuit die.

30. The method as recited in claim 29 wherein the circuit element is formed at least partially in the redistribution layers.

31. The method as recited in claim 29 wherein the redistribution layers are formed above a passivation layer of the integrated circuit die.

32. The method as recited in claim 29 wherein the redistribution layers are formed above integrated circuit pads.

33. The method as recited in claim 29 wherein the circuit element is formed below a passivation layer of the integrated circuit die.

34. The method as recited in claim 29 further comprising:
shielding using via structures stacked in the redistribution layers.

35. The method as recited in claim 29 further comprising:
shielding using via structures staggered in the redistribution layers.

36. The method as recited in claim 29 further comprising:
providing the circuit element spaced from the electrically conductive enclosure sufficiently spaced to limit the capability of the electrically conductive enclosure from generating an electromagnetic field that counteracts an electromagnetic field generated by the circuit element.

37. The method as recited in claim 29, further comprising:
effectively shielding with the electromagnetic shielding structure the circuit element from electromagnetic signals of particular frequencies generated by external elements.

38. The method as recited in claim 29, further comprising:
effectively preventing electromagnetic signals of particular frequencies generated by the circuit element from effecting external elements using the electromagnetic shielding structure.

39. The method as recited in claim 29 wherein the circuit element is an inductor structure.

40. A computer-readable medium encoding an integrated circuit product comprising:

at least one inductor structure formed on an integrated circuit die; and

an electromagnetic shielding structure formed at least partially in redistribution layers as part of the integrated circuit die, the electromagnetic shielding structure substantially surrounding the circuit element and wherein the circuit element is formed at least partially in redistribution layers.

41. A method of manufacturing an integrated circuit product comprising:

forming an electromagnetic shielding structure at least partially in one or more redistribution layers formed on an integrated circuit die, the electromagnetic shielding structure substantially surrounding a circuit element.

42. The method as recited in claim 41 further comprising:

forming the circuit element at least partially in the redistribution layers.

43. The method as recited in claim 41 further comprising:

forming a passivation layer.

44. The method as recited in claim 43 further comprising:

forming the redistribution layers above the passivation layer of the integrated circuit die.

45. The method as recited in claim 41 further comprising:

forming integrated circuit pads; and

forming the redistribution layers above the integrated circuit pads.

46. The method as recited in claim 41 wherein the circuit element is formed at least partially below a passivation layer of the integrated circuit die.

47. The method as recited in claim 41 wherein the electromagnetic shielding structure comprises an electrically conductive enclosure having a top plate, a bottom plate, and sidewalls.

48. The method as recited in claim 47 further comprising:
forming at least one of the top plate or bottom plate of the electrically conductive enclosure in under bump metal.

49. The method as recited in claim 47 further comprising:
forming the sidewalls of the electromagnetic shielding structure at least in part in under bump metal.

50. The method as recited in claim 47 further comprising:
forming the top plate and at least a portion of the sidewalls in under bump metal.

51. The method as recited in claim 50 further comprising:
forming via structures in the redistribution layers, the via structures supporting the top plate.

52. The method as recited in claim 41 wherein the redistribution layers include at least one redistribution metal layer and at least one redistribution dielectric layer.

53. The method as recited in claim 52 wherein the redistribution metal layer includes at least one of aluminum and copper.

54. The method as recited in claim 52 wherein the redistribution dielectric layer is at least 5um thick and wherein a dielectric layer of the integrated circuit die is less than 1um thick.

55. The method as recited in claim 54 wherein the redistribution dielectric layer is at least 15 um thick.

56. The method as recited in claim 47 further comprising:

forming the sidewalls of the electromagnetic shielding structure at least in part with via structures in the redistribution layers.

57. The method as recited in claim 56 wherein the via structures are stacked in the redistribution layers.

58. The method as recited in claim 56 wherein the via structures are staggered in the redistribution layers.

59. The method as recited in claim 41 wherein the circuit element comprises an inductor structure.

60. The method as recited in claim 41 wherein the circuit element comprises a capacitor structure.

61. An integrated circuit comprising:

means for electrically coupling nodes of an integrated circuit;

means for routing as part of the integrated circuit die an electrical connection between a contact pad on an integrated circuit die and a location of a package contact; and

means for electromagnetically shielding the coupling means with a structure formed at least partially by the means for routing.

62. The apparatus as recited in claim 61 further comprising:

means for reducing an electromagnetic field in the shielding means that counteracts an electromagnetic field generated by the coupling means.

63. An integrated circuit comprising:

an inductor formed in redistribution layers; and

means for shielding the inductor utilizing at least a first portion of a redistribution layer.